LUDLUM MODEL 2350-1
DATA LOGGER
Calibration Routines,
Parts List, and Schematics
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LUDLUM MEASUREMENTS, INC.
501 OAK ST., P.O. BOX 810
SWEETWATER, TX 79556
915/235-5494; FAX: 915/235-4672

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1. INITIAL INSTRUMENT CALIBRATION

1.1 Equipment Required

All instruments used in calibrating the Model 2350-1 must be calibrated by standards traceable to the National Institute of Standards and Technology and must have a current calibration label attached.

1. Ludlum Model 500 Pulser.
2. High Impedance voltmeter with at least 1000 megohms meter resistance and an accuracy of 0.5%.
3. Overload simulator (1000 megohm resistor).

1.2 Instrument Calibration

The following procedures will calibrate the electronics only. To program the instrument please refer to section 6. OPERATING INSTRUCTIONS of the Model 2350-1 Data Logger Manual.

WARNING:

The following procedures require that the instrument be re-initialized. This will clear all logged data and return all programmable settings to their default values. **DETECTOR SETUPS AND LOGGED DATA WILL BE PERMANENTLY LOST.**

1. Turn the Model 2350-1 ON. The display will temporarily go black and then the following two displays will appear for a few seconds each. Then the display that was active when the instrument was turned off will appear.

MEMORY TEST OK
CPU TEST OK

BATTERY VOLTAGE

BAT = 6.3

2. Re-initialize the instrument by entering the cold initialize command (**SSR**).
3. Check the battery voltage on the parameters display (**SVD1**). If it reads below 5.5 volts replace the batteries with fresh alkaline batteries and proceed.

Threshold and Window Calibration

4. Change the display time base to minutes (**SB1**) display units to counts (**SU7**), and the threshold to 100 (**T100**).
5. Turn the Model 500 Pulser polarity switch to the negative position.
6. Set the pulse amplitude range selector to the 50 mV position, and the LO-HI control to the maximum clockwise position.
7. Set the pulse frequency multiplier to the 1k position and adjust the pulse frequency so that the output is 400k cpm.
8. Connect the Model 2350-1 to the Pulser and verify that the ratemeter reads between 392-408kC/m.
9. Adjust the pulser amplitude control until the meter reads approximately 10 mV. The ratemeter display should read approximately 75% of the count input (**300 kC/m**).

1. INITIAL INSTRUMENT CALIBRATION

10. If the instrument does not read approximately 300 kC/m adjust the gain pot (R10) on the main board until it reads properly.

NOTE: The instrument threshold is now set at 100 = 10 mV

11. Turn the window ON (**WON**), and set it to 100 (**W100**).
12. Adjust the pulse amplitude control until it reads approximately 20 mV. The ratemeter reading should again indicate approximately 75% of the counts (**300 kC/m**).
13. Adjust the threshold setting to 200 (**T200**), 300 (**T300**), and 400 (**T400**) repeating the above procedure each time to verify that the threshold and window settings are linear.
14. Turn the window off (**WOFF**) and reset the threshold to 100 (**T100**).

High Voltage Calibration

15. Disconnect the instrument from the pulser and connect it to a high impedance voltmeter.
16. Set the high voltage to 1500 volts (**H1500**).
17. If the voltmeter does not read from 1498 - 1502 volts adjust the HV pot (**R52**) on the main board until it reads within tolerance.
18. Adjust the high voltage to 500 volts (**H500**). The voltmeter should read between 490 - 510 volts.
19. Adjust the high voltage to 2000 volts (**H2000**). The voltmeter should read between 1940 - 2060 volts.

Overload Calibration

21. Disconnect the instrument from the voltmeter, and connect it to the overload simulator resistor box.
22. Change to the Alarm Display (**SVD3**).
23. Turn the overload on (**OON**), and set it to 15.0 µA (**O150**).
24. Change to the Parameter Display (**SVD1**).
25. Set the high voltage to 1500 volts (**H1500**).
26. Change to the Main Display (**SVD0**). The ratemeter display at the top of the screen should be alternating between the ratemeter display and the word OVERLOAD at approximately 1 second intervals.
27. If this is not occuring adjust the OVERLOAD pot (**R7**) on the main board until the display alternates properly.
28. Adjust the high voltage to 1000 volts (**H1000**). The overload indicator should stop appearing.
29. Adjust the overlaod to 10.0 µA (**O100**). The OVERLAOD indicator should again begin to alternate with the ratemeter indicator.
30. Repeat steps 28 and 29 again with a voltage setting of 500 (**H500**) volts and an overload setting of 5 µA (**O50**).
31. When properly completed turn the overload alarm off (**OOFF**).

1. INITIAL INSTRUMENT CALIBRATION

1.2 Instrument Calibration (cont.)

Alarm Checkout

1. Connect the Model 2350-1 to the pulser.
2. Set the pulse frequency to 600k cpm.
3. Select the Alarm Display (**SVD3**).
4. Set the integrated dose alarm to 100k cpm (**P1E5**).

NOTE: If an alarm is indicated press the ACK/SCRL button to silence the audio.

5. Select the Main Display (**SVD0**) and zero the integrated dose (**SIZ**). The Integrated dose counter should start counting immediately and an alarm should be indicated when it reaches 100k cpm. After the alarm press the ACK/SCRL button to silence the audio.
6. Select the Alarm Display(**SVD3**) and set the scaler alarm to 60,000 counts (**K60000**).
7. Return to the Main Display (**SVD0**), set the scaler count time to 6 seconds (**F6**), and take a scaler count (**C**). When the scaler reaches 60,000 counts an alarm should again be indicated. Press the ACK/SCRL button again to silence the audio.
8. Adjust the pulse frequency of the pulser to less than 600k cpm.
9. Select the Alarm Display (**SVD3**) and set the ratemeter alarm to 600k cpm (**J6E5**).
10. Select the Main Display (**SVD0**) and readjust the pulse frequency to a setting of 600k cpm. The ratemeter alarm should be triggered. Press the ACK/SCRL button to silence the audio.
11. Verify that the ratemeter (**RAT**), scaler (**SCL**), and integrated dose (**DOS**) indicators are all alternating with the alarm (**ALM**) indicators at 1 second intervals.
12. Select the alarm display (**SVD3**)
13. Set all of the alarms to their default high settings (ratemeter, **J1E9**; scaler, **K1000000**; integrated dose, **P1E9**)
14. Select the Main Display (**SVD0**) and reset all of the alarm indicators (**X**).
15. Disconnect the instrument from the pulser and place it into the instrument can.

The electronics have now been calibrated and functionally checked. All remaining calibration procedures involve setting the programmable parameters of the instrument and are covered in the Model 2350-1 Data Logger Instruction Manual.

2. CALIBRATION ROUTINES

SOURCE PARAMETERS AND TYPICAL VALUES FOR MODEL 2350-1 CALIBRATIONS

To insure that the proper sized sources are used in calculating the calibration constant, and dead time of the Model 2350-1 and detectors the following calculation should be performed.

% Dead Time Loss = No. of source counts in 1 second X Dead Time (in seconds)

The following list provides some typical LO and HI cal points and dead times for various detectors:

TYPICAL DEAD TIME CALIBRATION, AND OVERLOAD POINTS

DETECTOR	LOW POINT	HIGH POINT	OVERLOAD POINT
44-2	500 μR/hr	15 mR/hr	100 mR/hr
44-6	20 mR/hr	400 mR/hr	1 R/hr
44-7	5 mR/hr	100 mR/hr	N/A
44-9	6 mR/hr	200 mR/hr	1 R/hr
44-38	20 mR/hr	400 mR/hr	1 R/hr
44-116	6 mR/hr	60 mR/hr	N/A

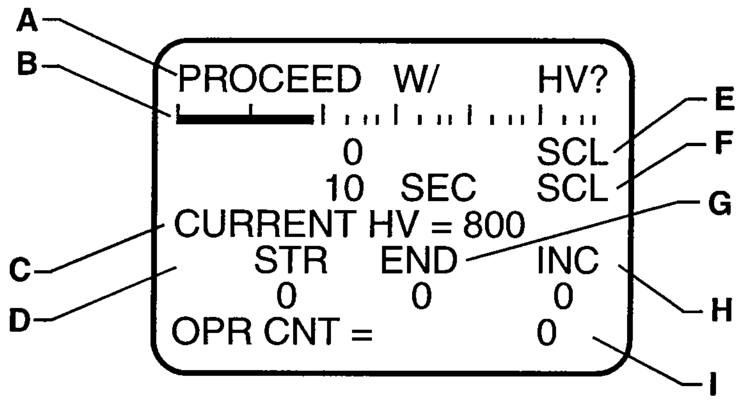
TYPICAL DEAD TIME AND CALIBRATION CONSTANT SETTINGS

DETECTOR	DEAD TIME	CALIBRATION CONSTANT
44-2	15 - 25 μsec.	$1.0e^{10}$ - $0.3e^{10}$
44-6	65 - 135 μsec.	$7.09e^{7}$ - $0.65e^{7}$
44-7	250 - 270 μsec.	$1.39e^{8}$ - $0.1e^{8}$
44-9	50 - 120 μsec.	$2.0e^{8}$ - $0.3e^{8}$
44-38	65 - 135 μsec.	$7.09e^{7}$ - $0.65e^{7}$
43-68 Alpha	15 - 25 μsec.	1
43-68 Beta	18 - 26 μsec.	1
43-37 Alpha	18 - 20 μsec.	1
43-37 Beta	19 - 25 μsec.	1

2. CALIBRATION ROUTINES

2.1 High Voltage Ramp Routine

The high voltage ramp routine is useful when a user needs to plateau a detector to determine the proper operating voltage of the detector. The following display will appear when performing the routine.



HIGH VOLTAGE RAMP ROUTINE DISPLAY

A. INFORMATION PROMPT: Prompts the user for the parameters required for the ramping routine. When the routine is first started the prompt will ask if the user wants to proceed with the current parameters. If answered YES the instrument will then prompt the user to begin the routine by executing the scaler count command. If answered NO then the following information prompts will appear immediately after the one before is answered.

Starting HV ?
Ending HV?
HV Increment?

The message DUMPING HEADER will then appear momentarily followed by the command "Ent C to start".

B. RATEMETER BARGRAPH DISPLAY: A logarithmic display of the ratemeter reading in cps.

C. HV IDENTIFIER: Identifies the current HV setting.

D. STR: Identifies the starting voltage of the HV ramping routine.

E. SCALER COUNT: Shows the scaler reading in progress.

F. SCALER TIMER: Shows the count time for the scaler. When a count is in progress the timer will show the time remaining in the count.

G. END: Identifies the ending HV setting for the ramping routine.

H. INC: Identifies the increment the voltage will be increased by in each step of the routine.

I. OPR CNT: Identifies the count at the beginning knee of the plateau or the recommended operating voltage.

2. CALIBRATION ROUTINES

The following example demonstrates how to run a plateau on a Model 44-2 Gamma Scintillator.

<u>KEYSTROKES</u>	<u>RESPONSE</u>

Note: Before performing the SHR(x) command, certain parameters must be set. The parameters that need to be set include the threshold, window position, and count time.

SHR(x) ENTER Where (x) = the number 0 or 1. 0 = Disables data dump to the serial port. 1 = Enables data dump to the serial port.	The Model 2350 display will show the detector display with the current set of detector parameters. There will be no prompt but you will need to select a set of parameters to use in the routine. If the current parameters are correct press "Y ENTER", otherwise select the set of detector parameters that you want to use and then press "Y ENTER". The instrument will proceed with the routine by displaying the screen shown on the opposite page.
N ENTER	This answers the prompt "PROCEED W/ HV" allowing the user to change the parameters of the routine.
500 ENTER	This set the beginning high voltage at 500 volts.
1000 ENTER	This sets the ending high voltage at 1000 volts.
25 ENTER	This sets the HV increment to 25 volts. (This increment is the amount that the high voltage setting will change between each step of the ramping routine.)
C ENTER	This activates the routine by starting the scaler counting.

"SHR0" will run the plateau routine, determine the operating votage, but will not dump data to the RS-232 port. "SHR1" will run the plateau routine, determine the operating voltage, and will dump the voltage setting and scaler count at each increment of the plateau routine.

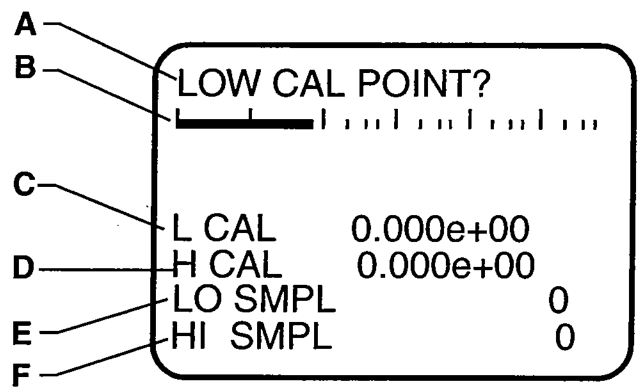
When the routine is complete the following prompt will appear:
"SAVE? HV = XXX"

"Y ENTER" will save the voltage as the operating voltage of the detector and the instrument will return to the screen that was active prior to the exucution of the routine. "N ENTER" will return to the screen that was active prior to the exucution of the routine without saving the voltage.

2. CALIBRATION ROUTINES

2.2 Calibration Constant and Dead Time Calibration with Background Subtract

This routine will use a two point (low-hi) method to calculate the calibration constant and dead time of the detector. The following display will appear when performing the routine.



CALIBRATION CONSTANT/DEAD TIME ROUTINE DISPLAY

A. INFORMATION PROMPT: Prompts the user for the parameters required for the routine. When the routine is first started the prompt will prompt the user low calibration point. Once entered it will prompt for the following parameters in order.

HI CAL POINT
TAKE BACKGROUND
TAKE LOW SAMPLE
TAKE HI SAMPLE
SAVE NUMBERS?

B. RATEMETER BARGRAPH DISPLAY: A logarithmic display of the ratemeter reading in cps.

C. L CAL: Identifies the low calibration point that will be used in the routine.

D. H CAL: Identifies the high calibration point that will be used in the routine.

E. LO SMPL: Shows the reading obtained from the low sample source.

F. HI SMPL: Shows the reading obtained from the high sample source.

NOTE: Line 1 will indicate the ratemeter reading when a sample is being taken, and lines 3 and 4 will show the scaler taking a count. When the routine is complete Line 3 will display the calculated calibration constant, and line 4 will show the calculated dead time constant. These numbers will be saved into the active detector setup if the user answers yes to the prompt to save the numbers.

2. CALIBRATION ROUTINES

The following example will calculate the cal constant and dead time of a Model 44-2 Gamma Scintillator in R/hr.

KEYSTROKES	RESPONSE
SKB ENTER	The Model 2350-1 will show the calibration constant/dead time routine with background subtract control display with a prompt to set the low cal point.
5e-4 ENTER	This will set the lower calibration point at 500 μR/hr, then a prompt will appear for the hi cal point.
15e-3 ENTER	This will set the high calibration point at 15 mR/hr, then a prompt will appear to take a background sample.
C ENTER	This will initiate the scaler to take a background reading, then a prompt will appear to take the low sample count. Place a 1 μCi ^{137}Cs check source on the end of the detector.
C ENTER	This will initiate the scaler to take a count with the low sample source, then a prompt will appear for the hi sample count. Place a 5 μCi ^{137}Cs check source on the end of the detector.
C ENTER	This will initiate the scaler to take the hi sample reading.

NOTE: The SSK command initiates the same routine as stated above except that the background count is not taken or considered when determining the calibration constant and dead time of the system.

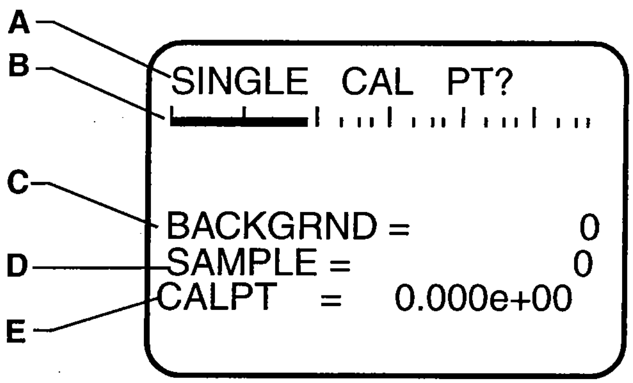
ADDITIONAL PARAMETERS

1. The background count should be less than 2% of the low sample count.
2. The low sample count should have at least 15,000 counts.
3. The high sample should be at least 100 times the low sample and produce between 30 - 60% dead time loss.

2. CALIBRATION ROUTINES

2.3 Single Point Calibration Constant Routine with Background Subtract

This routine will use a single point method to calculate the calibration constant of the detector. The following display will appear when performing the routine.



CALIBRATION CONSTANT/DEAD TIME ROUTINE DISPLAY

A. INFORMATION PROMPT: Prompts the user for the parameters required for the routine. When the routine is first started the prompt will prompt the user single calibration point. Once entered it will prompt for the following parameters in order.

TAKE BACKGROUND
TAKE SAMPLE
SAVE CAL CNST?

B. RATEMETER BARGRAPH DISPLAY: A logarithmic display of the ratemeter reading in cps.

C. BACKGRND: Identifies the background reading obtained during the routine.

D. SAMPLE: Identifies the sample count taken during the routine.

E. CALPT: Identifies the reference calibration point set for the routine.

NOTE: Line 1 will indicate the ratemeter reading when a sample is being taken, and lines 3 and 4 will show the scaler taking a count. When the routine is complete Line 8 will display the calculated calibration constant. This number will be saved into the active detector setup if the user answers YES to the prompt to save the number.

2. CALIBRATION ROUTINES

The following example will calculate the cal constant of a Model 44-2 Gamma Scintillator in R/hr.

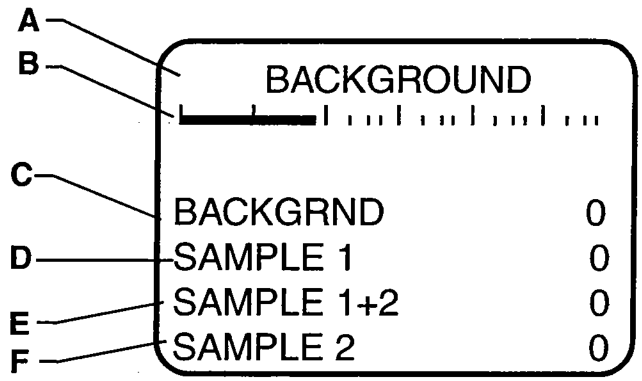
KEYSTROKES	RESPONSE
SSB ENTER	The Model 2350-1 will show the single point calibration constant routine with background subtract control display with a prompt to set the single cal point.
5e-4 ENTER	This will set the single calibration point at 500 µR/hr, then a prompt will appear to take a background reading.
C ENTER	This will initiate the scaler to take a background count, then a prompt will appear for the sample count. Place the detector in a 500 µR/hr field.
C ENTER	This will initiate the scaler to take the single sample reading.

NOTE: The SSS command initiates the same routine as stated above except that the background count is not taken or considered when determining the calibration constant.

2. CALIBRATION ROUTINES

2.4 Two Source Dead Time Calibration Routine with Background Subtract

This routine will use a single point method to calculate the calibration constant of the detector. The following display will appear when performing the routine.



CALIBRATION CONSTANT/DEAD TIME ROUTINE DISPLAY

A. INFORMATION PROMPT: Prompts the user for the parameters required for the routine. When the routine is first started the prompt will appear for the background count. Once entered it will prompt for the following parameters in order.

SAMPLE 1
SAMPLE 1+2
SAMPLE 2
SAVE DEAD TIME?

B. RATEMETER BARGRAPH DISPLAY: A logarithmic display of the ratemeter reading in cps.

C. BACKGRND: Identifies the background count taken during the routine.

D. SAMPLE 1: Identifies the sample count taken with source 1 during the routine.

E. SAMPLE 1 +2: Identifies the sample count taken with sources 1 & 2 during the routine.

F. SAMPLE 2: Identifies the sample count taken with source 2 during the routine.

NOTE: Lines 3 will show a timer and line 4 will show the word COUNTING when a count is in progress. When the routine is complete Line 3 will display the calculated dead time for the detector. This number will be saved into the active detector setup if the user answers YES to the prompt to save the number.

2. CALIBRATION ROUTINES

The following example will calculate the dead time of a Model 44-2 Gamma Scintillator in R/hr.

KEYSTROKES	RESPONSE
SSD ENTER	The Model 2350-1 will show the dead time calibration routine with background subtract control display with a prompt to take a background reading.
C ENTER	This will initiate a count to get a background sample, then a prompt will appear to take a reading from sample 1.
C ENTER	This will initiate count for sample 1, then a prompt will appear for a count with samples 1 & 2.
C ENTER	This will initiate a count of samples 1 & 2 together, then a prompt will appear for a count with sample 2 only.
C ENTER	This will initiate a count of sample 2 only.

ADDITIONAL PARAMETERS

1. The sources used for this test should be approximately the same size and each should provide a minimum of 25,000 cpm.
2. When combined the sources must provide a between 25 - 60% dead time loss.

3. THEORY OF OPERATION

3.1 AMPLIFIER/POWER SUPPLY BOARD #5371-002

3.1.1 INPUT

Negative going pulses are coupled from the detector through C9 to emitter follower Q1. CR6 is a voltage reference which provides a bias voltage of approximately +3.3 Vdc to Q1 via R45. R9 protects Q1 from input inadvertent shorts/ transients. R40 couples the detector to the high voltage supply (HV).

3.1.2 AMPLIFIER

U3 is a self-biased amplifier which provides gain in proportion to R12 divided by the series combination of R11 and R10. R10 is adjusted to provide a pulse height in proportion to a given threshold setting at comparator U4 (typically adjusted to trigger with a detector input pulse of 10 millivolts at a threshold setting of 100). Transistor (pins 4, 5, and 6 of U3) provide amplification and pulse polarity inversion. Transistor pins 10 through 15 are coupled as a constant current source to pin 6 of U3. The output self-biases to 2 Vbe — approximately 1.4 Vdc at pin 7 of U3. This provides just enough bias current through pin 6 to conduct all of the current from the constant current source. Positive pulses from pin 7 are coupled to the Window and Threshold comparators, U4.

3.1.3 WINDOW/THRESHOLD

Threshold (THR) comparator, pins 5, 6, and 7 of U4, provides the lower pulse height discrimination. Pulses are AC coupled from amplifier U3 via C23 to pin 6 of U4. THR reference voltage data from the microprocessor board (µP) is processed by digital to analog convertor (DAC) U6 and coupled to pin 5 of U4 via opamp U5. R54 and C13 provide additional filtering of the reference voltage. THR reference Vdc is approx. +122 millivolts (mV) with the THR set at 100 on display — 1.222 Vdc at a THR setting of 1000. As the pulse height at pin 6 of U4 increases above the reference voltage at pin 5, pin 7 — normally high (approx. +5 Vdc) goes low for the pulse duration.

Window (WIN) comparator, pins 1, 2, and 3 of U4 provide the upper pulse height discrimination. Pulses are coupled from amplifier U3 to pin 2 of U4. WIN reference voltage data from the µP is processed by DAC U6 and coupled to pin 3 of U4. Q2 applies approx. +5 Vdc to the WIN reference to disable the WIN comparator when the WIN OFF signal is applied to the base of Q2. The WIN reference voltage rides on top of the THR reference — i.e., with a THR and WIN setting of 100, the WIN reference at pin 3 of U4 will equal approx. +122 mV referenced above the THR at pin 5 or approx. +244 mV referenced to chassis ground. If the THR is increased to 200 and the WIN still remains at 100 the WIN reference will still equal approx. +122 mV referenced to the threshold but will increase to approx. +366 mV when referenced to ground (THR = 244 mV + 122 mV WIN = 366 mV). As the pulse amplitude increases above the WIN reference voltage, pin 1 of U4 goes low for the pulse duration.

3.1.4 WINDOW/THRESHOLD LOGIC CIRCUIT

Negative pulses from the THR comparator are coupled to univibrator U9. Negative, pulses (approx. 5 volt) are present at univibrator output pin 7 of U9 (PULSE') as long as pins 13 and 3 remain high. When a WIN pulse is present at pins 13 and 3 the **R**eset function is enabled which disables the PULSE' output locking pin 7 high. Pulses are connected from pin 7 to the µP on the Central Processor Board for count processing. Pin 7 is tied back to pin 13 via CR1 to provide a time delay (approx. 8 to 10 µs) for the µP clock cycle to complete before the next pulse can be recognized by the micro-processor.

3.1.5 DIGITAL TO ANALOG CONVERTORS

U6 and U7 are digital to analog convertors (DAC) which convert the digital data from the µP to analog signals to control the THR, WIN, High Voltage Reference (HV REF), and Overload Reference (OVR REF) variables. Data via BUS0-BUS3 and A0-A2 is loaded into the DAC latches for U6 and U7 by strobing CE3' and CE4' (Chip Select). CE5' (Up Date) is then strobed to transfer the data stored in the latches to the DAC outputs.

3.1.6 HIGH VOLTAGE SUPPLY AND DETECTOR OVERLOAD

Detector High Voltage (HV) is developed by blocking oscillator Q3, T1, C29 and rectified by voltage multiplier CR3-CR5, CR14, CR15, C5, C32, C37, and C38. Q4, CR13, and R41 provide a regulated voltage of approx. 4.4 Vdc (battery voltage must be +4.4 Vdc) to the emitter of Q3. HV increases as current through Q5 increases with maximum output voltage with Q5 saturated.

HV is coupled back through R5, through voltage follower U1, to pin 6 of U2 to complete the regulation loop. Resistors R52 and R6 complete the HV divider network to ground. HV regulation is produced by opamp comparator pins 5, 6, and 7 of U2. During stable operation the voltage at pin 6 will equal pin 5. If HV REF is increased, pin 7 of U2 will increase increasing conduction of Q5 until the voltage at pin 6 equals pin 5 of U2 via HV divider network, R5, R52, and R6. R52 is adjusted to calibrate the HV output to the HV REF signal supplied to pin 5 of U5 by the DAC — HV REF is set at approx. 1500 mV by entering the "H1500" command into the Model 2350-1, the HV CAL is adjusted for 1500 Vdc at the detector connector. C1-C3, C8-C7, C19, and C27 provide additional filtering of the HV output.

Detector Overload is achieved by measuring the voltage differential across R4. As current is increased into the detector, a voltage drop is produced across R4. The HV on either side of R4 is converted to a low voltage by resistor divider networks R5, R52, R6, and R44, R7, and R43. The voltage differential is coupled to differential opamp, pins 12-14 of U1, via opamp buffers. The differential output is coupled to opamp comparator, pins 8- 10 of U1. OVR REF is provided by the µP via the DAC — OVERLOAD' is coupled back to the µP. R7, CURRENT CAL, calibrates the detector current drain to the OVR REF input — i.e., a 10µA load is connected to the detector output; the overload is set to "100" by entering the "O100" command (approx. 610mV at OVR REF), R7, CURRENT CAL, is then adjusted until pin 8 or U1 just starts to trigger low.

3.1.7 LOW VOLTAGE SUPPLY

Supply voltages of +5 and -10 Vdc are supplied by U8, T2, and supporting components. U8 is a switching regulator with an on-board comparator providing regulation. An internal voltage reference of 1.0 Vdc maintains the inverting and non-inverting comparators at 1.0V via the feedback loop. Oscillator frequency, set by C36, is approx. 100 kHz at pin 5 of U5. CR11 and C26 provide rectification and filtering for the +5V output. CR12 and C25 provide rectification and filtering for the -10V output.

U11 is a -2.5 Vdc voltage reference for the DAC's — U6 and U7. C8 located on the Backplane board maintains the battery voltage charge during inadvertent battery disconnection (mechanical shock).

3.1.8 LCD VIEWING ANGLE SUPPLY

U2 is configured as a differential opamp which controls the backplane voltage to adjust the viewing angle for the LCD graphics display. Output voltage, pin 1 of U2 is adjustable from 0 to -10 Vdc by varying R50 (VIEWING ANGLE). LCD backplane variance due to temperature is compensated by CR10.

3.2 CENTRAL PROCESSOR BOARD #5371-068

3.2.1 MICROPROCESSOR (μP)

U124, Intel 80C51FA, is the Model 2350-1 central processor. The μP clock frequency is crystal controlled by Y159 and related components at 6.144 MHZ. C172 resets the μP at power-up to initiate the start of the program routine. The main program routine is stored in EPROM, U122. User parameters and logged data is stored in the 8k X 8 RAM, U123. (replaced with 64k X 8 RAM located on the Memory Expander board)

Address and data information are multiplexed by latch U121 from the μP to the two memory chips. The low address bits A0-A7 are multiplexed with the data bus, BUS0-BUS7, out of the μP. U121 latches the address data AO-A7 on lines BUS0-BUS7 during the first part of the external memory cycle when the ALE input is strobed.

The HD175 ACCESS shunt configures the μP parameter access mode and password. When pins 1 and 2 are shunted (default) the access parameters is determined by the settings preset in the EPROM and the password entered in RAM. If shunt is placed between pins 2 and 3 the password is set to "0" and the access level is set to "3".

The ACKNOWLEDGE' input is pulled low when the front panel ACKNLDGE pushbutton switch is depressed silencing the audible alarm(s). The OVERLOAD' signal from the AMP/PS board instructs the μP to initiate an OVERLOAD condition. WIN OFF' is an output signal from the μP to the AMP/PS board which disables the Window feature.

The TONE' input comes from the I/O processor which toggles the TONE'/ALARM line low when the external bar code wand registers bar code information. The TONE' and ALARM' (μP output signal from pin 5 of U124) signals initiate an independent audible tone by changing the CV (control voltage) input on the ICM7556 timer, U118.

The READY, CLEAR SEND, RECEIVE, and XMIT data lines communicate the RS-232 and bar code reader wand information from/to the I/O processor to/from the central processor. The RESET output at pin 13 of U124 is coupled to the I/O board to reset the I/O processor. Q174 inverts the RESET signal (RESET') providing a reset line for the LCD graphics display. The PULSE' input supplies the pulses from the AMP/PS board to be counted and converted into data by the μP.

3.2.2 BATTERY VOLTAGE VFC

Un-switched (connected directly to batteries) battery voltage — +BATUNS — is divided by resistor divider network R148 and R149 and connected to voltage to frequency convertor (VFC), U125. VFC OUT is connected to a counter inside the μP which counts the frequency for a preset time converting to a number displayed on the LCD representing the battery voltage. R130, BAT CAL, adjusts the VFC frequency output to calibrate the LCD BAT reading to the actual battery voltage.

NOTE: Disregard sections 3.2.3 and 3.2.4 for the Model 2350-1

3.2.3 RECORDER DRIVE CIRCUIT

The RCDR output from the μP is coupled to MOSFET transistor Q126. The μP uses pulse-width modulation for the recorder signal. The pulse-modulated signal is integrated by R144 and C100. Pins 5, 6, and 7 of U126 "buffers" the integrated voltage from R131. R131 provides calibration of the recorder output voltage. Pins 1, 2, and 3 of U126 are configured as an opamp voltage follower providing recorder drive.

3.2.4 ADDRESS DECODER/VOLTAGE BACKUP

U120 is address decoder which generates the chip enable signals — CEO-CE7 — by monitoring address lines A13-A15. U120 also provides battery backup, +5VBACK, to the Clock chip U119 and the RAM U123. This enables the user to change the instrument batteries without losing RAM memory. +BATUNSR supplies battery voltage to CR112 voltage reference to limit the voltage at 5.1 Vdc. The 5.1 Vdc is coupled to a 0.1

farad capacitor through CR113. CR113 prevents C129 from discharging through the +BATUNSR line when the batteries are removed.

3.2.5 CLOCK CHIP

U119 provides the time and date information used in conjunction with the logged data. U119 is crystal controlled by Y158 and supporting components C102 and C103 at 32.786 kHz. The 10 Hz output at pin 13 of U119, provides the timing frequency to the µP.

3.2.6 AUDIO CIRCUIT

Pulses are coupled from the AMP/PS board to U128 — RDD 104 decade divider chip. AUDIO DIVIDE (front panel) by "1" switch position jumpers the PULSE' input directly to the CLICK' input to the timers. Divide by "10" and "100" switch positions connect the DIV OUT of U128 to the CLICK' input using U128 for pulse division. U118, a dual package 7555 timer, provides audio oscillation. Pulses (CLICK') are coupled to the first timer, pins 1-6 of U118, via C97. This timer is configured as a monostable multivibrator (one-shot) producing a fixed pulse-width for each input pulse at pin 6 of U118. Pulse-width is set by R161 and C95. CR114 limits pulse input to pin 6 of U118 to 5.6 volts; R134 is a pull-up resistor for the AC coupled pulse. The second half of U118 is configured as a astable (free-running) multivibrator which produces the audible tone — frequency is set by R133 and C96.

T157 provides amplification of the audio signal driving the unimorph speaker. Audio volume is varied by adjusting the voltage on top of the primary winding of T157 via the front panel volume control. When an ALARM' is initiated maximum voltage applied by saturating Q154.

3.3 I/O INTERFACE BOARD #5371-063

3.3.1 MICROPROCESSOR (µP)

U15, Intel 80C51FA, communicates and processes information bi-directionally from/to the RS-232 interface (U13) to/from the central processor via the serial interface lines XMIT, READY, RECEIVE, and CLEAR SEND. U15 also decodes information from the bar code reader (WAND) and sends information to central processor. The µP clock frequency is crystal controlled by Y159 and related components at 6.144 MHZ.

U14, EPROM, stores the program for the I/O µP. U14 incorporates on-board latches to separate the multiplexed address and data buss lines.

CR26-CR28 provide "clipping" of transients which may be produced at the SERIAL I/O port.

3.3.2 RS-232 INTERFACE

U13, MAX232, is a +5 Vdc powered RS-232 driver/ receiver used to interface the Model 2350-1 to a computer or keypad terminal. U13 incorporates on-board voltage multipliers which generate the +10 and -10 volts required for RS-232 communication.

3.3.3 BACKLIGHT DRIVE

The LCD backlight is illuminated by appling power to +EL POWER when front panel BACKLIGHT switch is ON. With battery voltage applied to +EL POWER, blocking oscillator — Q23, T1 and supporting components begin oscillating. The signal is amplified by T1 to provide a 70VAC signal to drive the LCD backlight. R30, a 10 ohm resistor, limits the power-up surge to the oscillator circuit.

3. THEORY OF OPERATION

3.4 64k MEMORY EXPANDER BOARD #5371-054

NOTE: When the MEMORY EXPANSION board is added, U120 (DS1211) and U123 (CDM6264) on the CENTRAL PROCESSOR board must be removed. The red entries in the CENTRAL PROCESSOR theory of operation should be removed/or inserted for the M2350-1.

U119 is a 128k RAM (only 64k is used) used to store user parameters and logged data. U119 is selected by the central μP by applying a logic "high" to the RAM input, Pin 30 of U119. The Recorder circuit is disabled on the Central Processor board and the RCDR output on the central μP is used to enable the Memory Expansion board RAM.

U117 is address decoder which generates the chip enable signals — CE1-CE7, E1 — for the DAC's on the AMP/PS board and the Clock chip on the Central μP board by monitoring address lines A12-A14 from the central μP.

U115 provides battery backup, +5VBACK, to the Clock chip (U119) on the Central μP board and the RAM. This enables the user to change the instrument batteries without losing the RAM memory. U115 also provides a RESET signal which goes low when the +5V supply to pin 2 of U115 drops below a preset threshold (4.5-4.75 volts). This opens U116 analog switches disabling the RAM and CLOCK' signals from the data bus to save the parameter and logging memory.

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

AMPLIFIER / POWER SUPPLY BOARD

Ref. No.	Description	Part No.
CAPACITORS		
C1-C3	0.0056µF, 3kV	04-5522
C4	0.1 µF	04-5521
C5	0.0015 µF, 3kV	04-5518
C6-C8	0.0056 µF, 3kV	04-5522
C9	100 pF, 3kV	04-5532
C10	10 µF	04-5592
C11-C12	100 pF	04-5527
C13	0.01 µF	04-5523
C14	47 pF	04-5533
C15	100 µF	04-5576
C16	220 pF	04-5530
C17	100 pF	04-5527
C18-C19	0.0056 µF, 3kV	04-5522
C20-C21	33 pF	04-5616
C22	0.01 µF	04-5523
C23	0.1 µF	04-5521
C24	0.0056 µF, 3kV	04-5522
C25	22 µF	04-5579
C26	220 µF	04-5639
C27	0.0056 µF, 3kV	04-5522
C28	100 pF, 3kV	04-5532
C29	0.01 µF	04-5523
C30	100 µF	04-5576
C31	100 pF	04-5527
C32	0.0015 µF, 3kV	04-5518
C33	33 pF	04-5616
C34	1 µF	04-5575
C35-C36	0.001 µF	04-5519
C37-C38	0.0015 µF, 3Kv	04-5518
C39	10 µF	04-5592
C40	0.1 µF	04-5521
C41	33 pF	04-5616
C42	0.01 µF	04-5523
DIODES		
CR1-CR2	1N4148	07-6272
CR3-CR5	MR250-2	07-6266
CR6	1N5226	07-6260
CR7	1N5819	07-6306
CR8-CR10	1N4148	07-6272
CR11-CR12	1N5819	07-6306
CR13	1N4148	07-6272

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

Ref. No.	Description	Part No.
DIODES		
CR14-CR15	MR250-2	07-6266
CR16-CR18	1N4148	07-6272
TRANSISTORS		
Q1	2N3904	05-5755
Q2	MPS6534	05-5763
Q3	MPS-U51	05-5765
Q4	MPS-U01	05-5778
Q5	2N3904	05-5755
RESISTORS		
R1	10kohm, 333MW	12-7748
R2	47 ohm, 333MW	12-7756
R3	56 kohm, 333MW	12-7789
R4	4.7 Mohm	10-7030
R5	1 Gohm	12-7686
R6	470 kohm, 333MW	12-7757
R7	1 Mohm, pot	09-6828
R8	100 kohm, 333MW	12-7747
R9	10 kohm, 333MW	12-7748
R10	100 kohm, pot	09-6823
R11	1 kohm, 333MW	12-7750
R12	470 kohm, 333MW	12-7757
R13-R14	10 kohm, 333MW	12-7748
R15	1 kohm, 333MW	12-7750
R16	4.7 kohm, 333MW	12-7755
R17-R19	10 kohm, 333MW	12-7748
R21	0.1 ohm, 3W	12-7647
R22	80.6 kohm, 333MW	12-7762
R23	1 Mohm, 333MW	12-7763
R24	10 Mohm, 333MW	12-7749
R25	10 kohm, 333MW	12-7748
R26	80.6 kohm, 333MW	12-7762
R27	62 kohm, 333MW	12-7790
R28	1 Mohm, 333MW	12-7763
R29	33.2 kohm, 333MW	12-7793
R30	47 kohm, 333MW	12-7758
R31	100 ohm, 333MW	12-7746
R32	221 kohm, 333MW	12-7792
R33-R36	10 kohm, 333MW	12-7748
R37	820 ohm, 333MW	12-7791
R38	10 kohm, 333MW	12-7764

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

Ref. No.	Description	Part No.
RESISTORS		
R39-R40	1 Mohm	10-7028
R41	100 kohm, 333MW	12-7747
R42	3 kohm, 333MW	12-7768
R43	470 kohm, 333MW	12-7757
R44	1 Gohm	12-7686
R45	100 kohm, 333MW	12-7747
R46	10 kohm, 333MW	12-7748
R47	33.2 kohm, 333MW	12-7793
R48	1 Mohm, 333MW	12-7763
R49	12 kohm, 333MW	12-7787
R50	1 kohm, pot	09-6831
R51	330 ohm, 333MW	12-7788
R52	1 Mohm, pot	09-6828
R53	22 kohm, 333MW	12-7754
R54	10 kohm, 333MW	12-7748
R55	1 kohm, 333MW	12-7750
R56	1 Mohm, 333MW	12-7763
R57	80.6 kohm, 333MW	12-7762
R58	1 Mohm, 333MW	12-7751
R59	10 kohm, 333MW	12-7748
RESISTOR NETWORK		
RN1	5.6 kohm	12-7696
RN20	220 kohm	12-7578
TRANSFORMERS		
T1	M2350-1 HVPS	4275-037
T2	M2350-1 LVPS	4275-089
INTEGRATED CIRCUITS		
U1	LT1079	06-6252
U2	LT1078	06-6251
U3	CA3096	06-6023
U4	TLC372	06-6265
U5	LT1078	06-6251
U6-U7	AD7549	06-6253
U8	LM2578	06-6223
U9	CD4098	06-6066
U10	LT1078	06-6251
U11	LM385Z	05-5791

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

CENTRAL PROCESSOR BOARD

Ref. No.	Description	Part No.
CAPACITORS		
C95	0.047 μF	04-5565
C96	0.001 μF	14-5519
C97	47 pF	04-5533
C98	0.01 μF	04-5523
C99-C100	0.1 μF	04-5521
C101	27 pF	04-5614
C102-C103	22 pF	04-5552
C104	27 pF	04-5614
C109	10 μF	04-5592
C110	100 μF	04-5576
C111	1 μF	04-5575
C129	0.1 F	04-5633
C172	10 μF	04-5592
C177	0.1 μF 100V	04-5521
DIODES		
CR112	1N5231	07-6261
CR113-CR115	1N4148	07-6272
CR162	1N4148	07-6272
HEADER		
HD175	3 PIN SIP	n/a
TRANSISTORS		
Q153	2N3904	05-5755
Q154	MPS6534	05-5763
Q155	2N3904	05-5755
Q168,Q174	2N7000	05-5820
RESISTORS		
R130	10 kohm, pot	09-6822
R131	100 kohm, pot	09-6823
R132	2.2 kohm	10-7012
R133	470 kohm	10-7026
R134	220 kohm	10-7066
R135	5.6 kohm	10-7042
R137-R138	10 kohm	10-7016
R139	33 kohm	10-7019
R140	10 kohm	12-7540
R141-R142	100 kohm	12-7557
R143	7.15 kohm	12-7620

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

Ref. No.	Description	Part No.
RESISTORS		
R144	1 Mohm	10-7028
R148	35.7 kohm	12-7640
R149	8.66 kohm	12-7623
R160	220 kohm	10-7066
R161	150 kohm	10-7024
R164	1 Mohm	10-7028
R166-R167	10 kohm	12-7540
R170	1 Mohm	10-7028
R176	220 kohm	10-7066
RESISTOR NETWORKS		
RN151	22 kohm	12-7566
TRANSFORMERS		
T157	M2221, 300-9	4275-074
INTEGRATED CIRCUITS		
U118	ICM7556	06-6244
U119	MM58274	06-6254
U120	CPL-200-T2-T	06-6441
U121	CD74HC573	06-6093
U122	27C512	06-6264
U123	CPL-140-T2-T	06-6439
U124	80C51FA	06-6236
U125	LM331	06-6156
U126	TLC27M71P	06-6248
U128	RDD104	06-6060
CRYSTALS		
Y158	32 kHz XTAL	01-5219
Y159	6.144 MHz XTAL	01-5212

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

64k MEMORY EXPANDER BOARD

Ref. No.	Description	Part No.
RESISTORS		
R001	22.1 kohm	12-7843
R114	221 kohm	12-7845
INTEGRATED CIRCUITS		
U115	MAX703ESA	06-6381
U116	CD74HC4066M	06-6323
U117	CD74HC138M	06-6339
U119	CXK581000M	06-6385

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

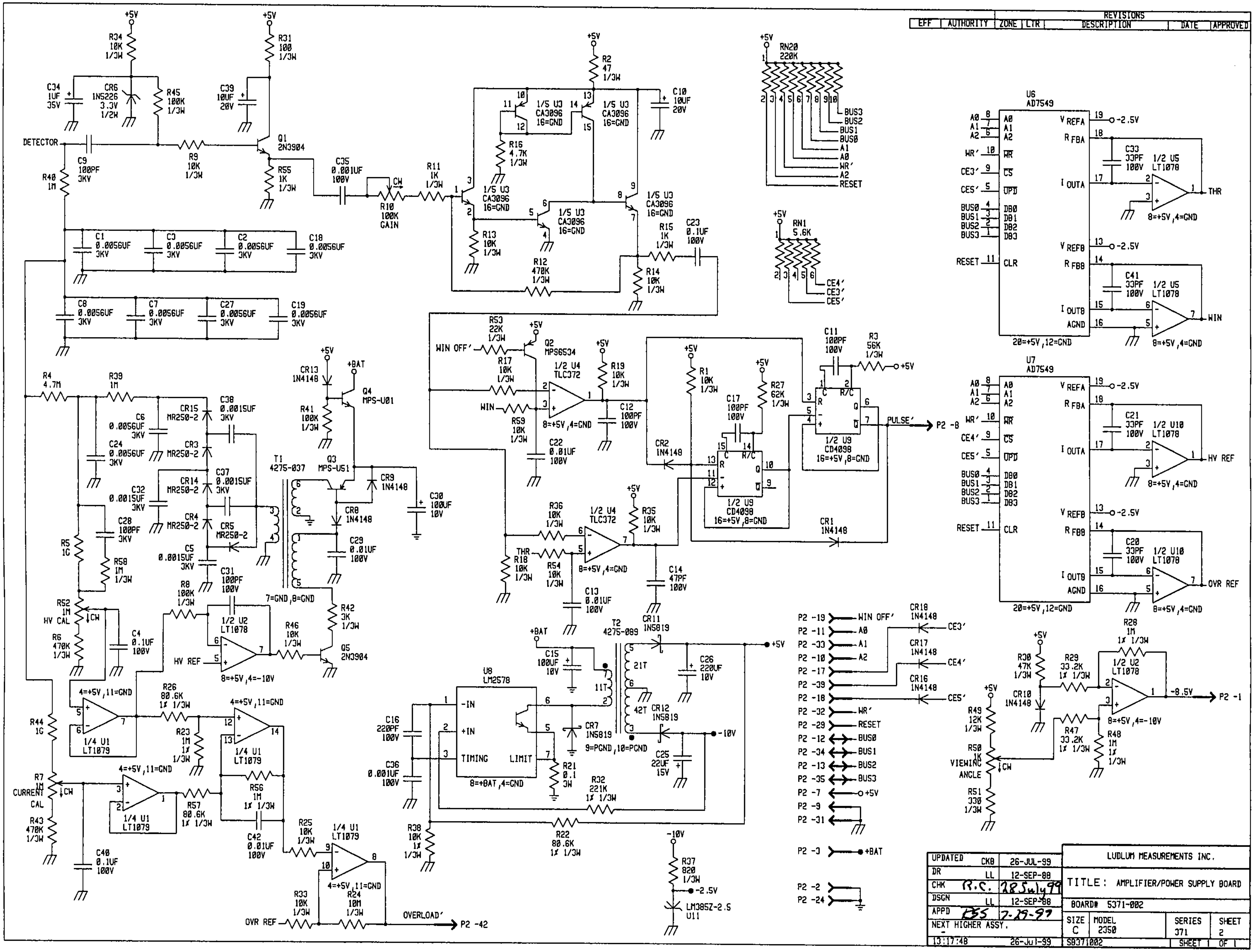
I/O INTERFACE BOARD

Ref. No.	Description	Part No.
CAPACITORS		
C3-C4	27 pF	04-5614
C5	0.047 µF	04-5565
C6	100 µF	04-5576
C8-C11	10 µF	04-5592
C12	4.7 µF	04-5578
C37-C39	220 µF	04-5639
RESISTORS		
R16	33 ohm	10-7001
R19	8.2 kohm	10-7015
R20-R21	3.3 kohm	10-7013
R30	10 ohm	10-7046
R40	4.7 ohm	10-7095
RESISTOR NETWORKS		
RN33	10 kohm	12-7777
DIODES		
CR26-CR28	1N5231	07-6261
TRANSISTORS		
Q23	2N3904	05-5755
TRANSFORMERS		
T1	M2350-1 EL	4275-090
INTEGRATED CIRCUITS		
U13	MAX232	06-6188
U36	87C51FA	06-6405
CRYSTALS		
Y25	6.144 MHz MICRO XTAL	01-5212

4. PARTS LIST, COMPONENT LAYOUTS, AND SCHEMATICS

BACKPLANE BOARD

Ref. No.	Description	Part No.
RESISTORS		
R6	1 kohm	10-7009
DIODES		
CR5	1N4148	07-6272
CR7	1N5819	07-6306
CONNECTORS		
J1-J2	125X44-CBNEARS EZA22DRSN	13-8181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BOARD# 5371-002
SIZE C
MODEL 2350
SERIES 371
SHEET 2
SHEET 1 OF 1
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DR LL 12-SEP-88
CHK R.C. 28 July 99
DSGN LL 12-SEP-88
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NEXT HIGHER ASSY.
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REVISIONS
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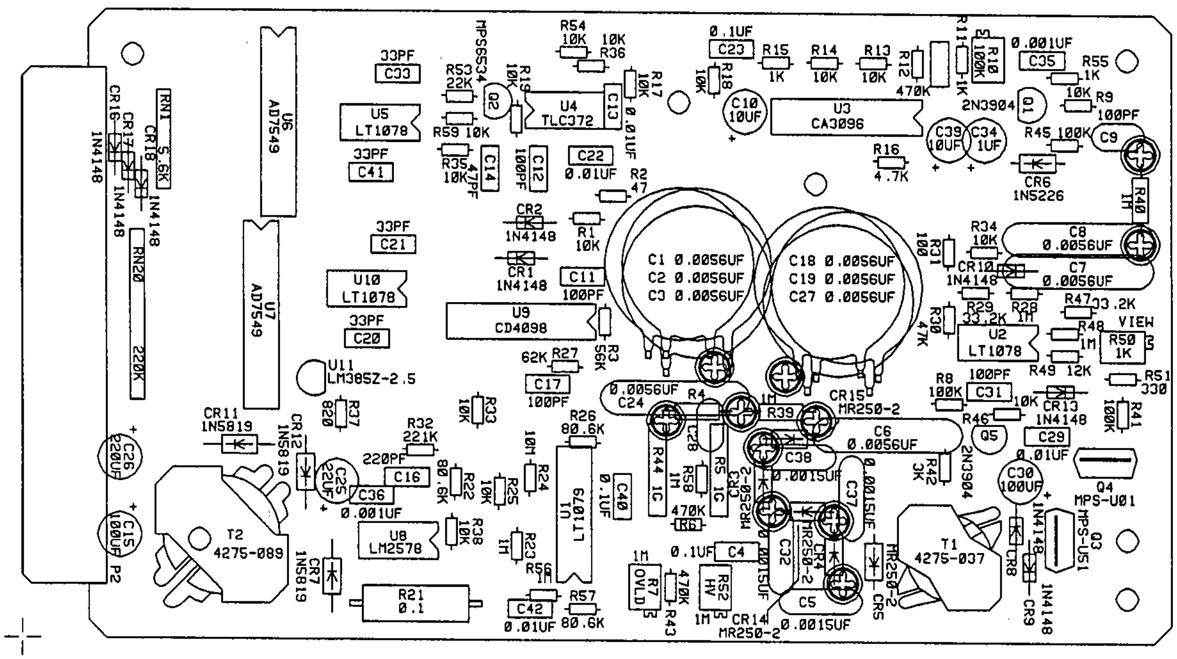

LUDLUM MEASUREMENTS INC.		SWEETWATER, TX.		
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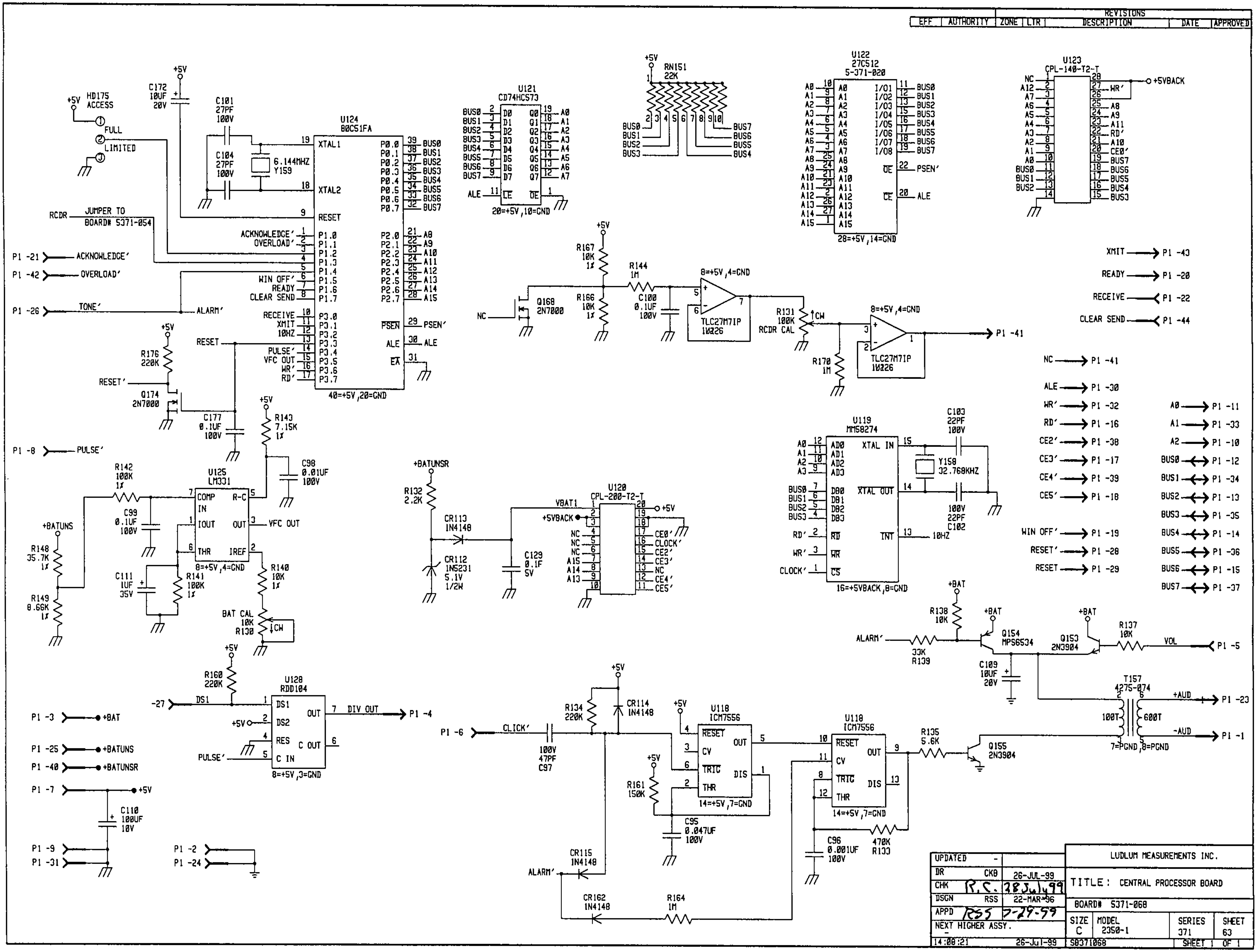
COMP PASTE □	COMP MASK □	SLDR PASTE □		SLDR MASK □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U125
LM331
U128
RDD104
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T157
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HD175
ACCESS
FULL
LIMITED
RCDR
JUMPER TO
BOARD# 5371-054
BAT CAL
RCDR CAL
UPDATED
DR
CKB
26-JUL-99
CHK
R.C.
28 July 99
DSGN
RSS
22-MAR-96
APPD
RSS
7-29-99
NEXT HIGHER ASSY.
14:08:21
26-Jul-99
LUDLUM MEASUREMENTS INC.
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SIZE
C
MODEL
2350-1
SERIES
371
SHEET
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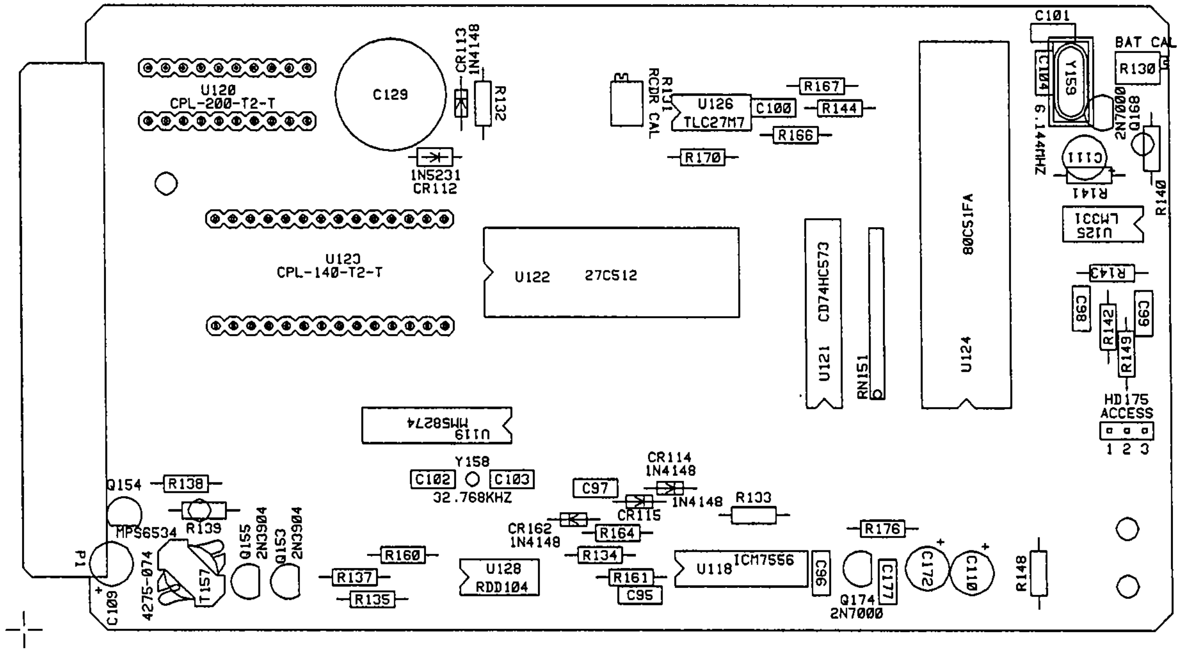

LUDLUM MEASUREMENTS INC. SWEETWATER, TX.			
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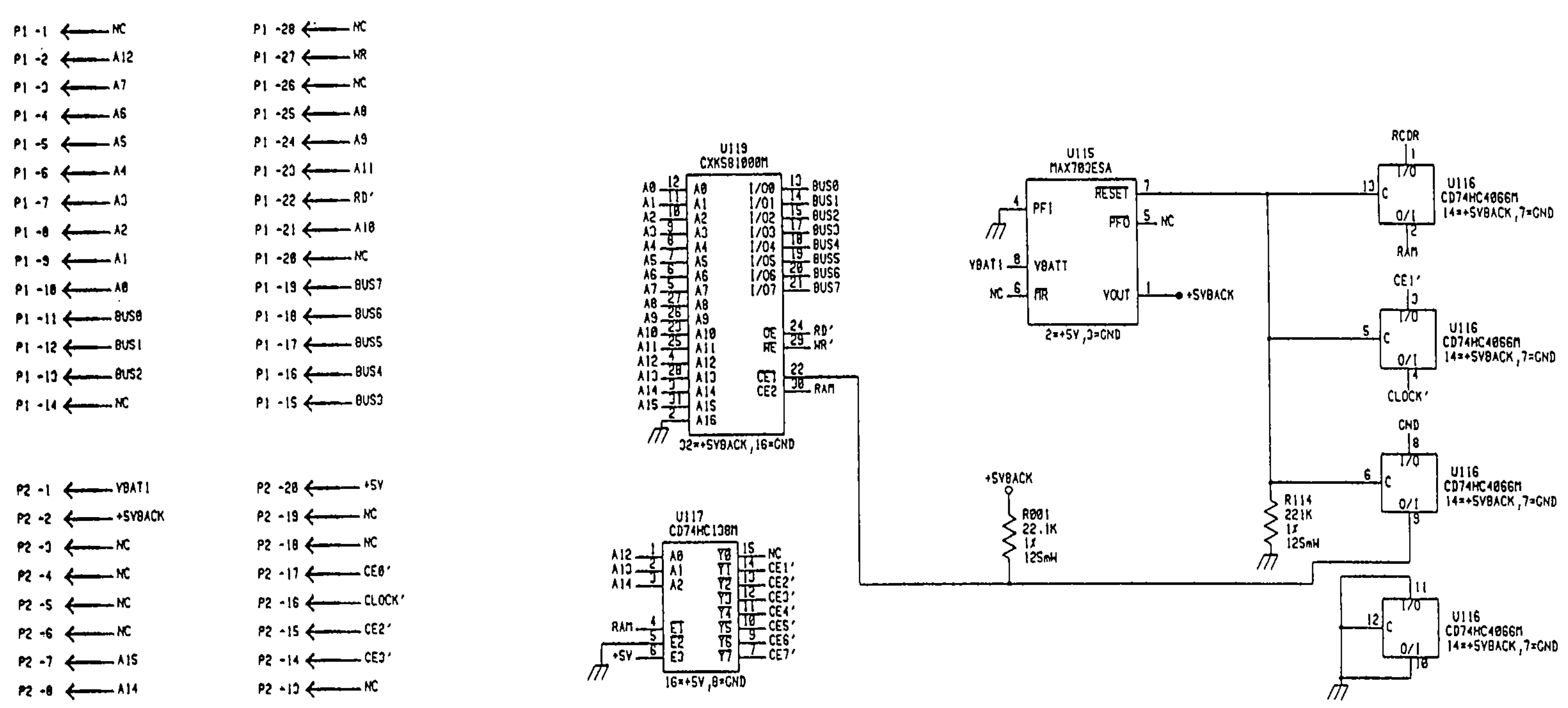
CHK R.C.	July 28 99	BOARD: 5371-068	
DSGN RSS	09/17/96	MODEL: 2350-1	
APP RSS	7-29-99	FILENAME: BS371068	
COMPONENT	SOLDER	16:31:18	28-Jul-99
OUTLINE	OUTLINE	REVISION 1.0	SERIES 371 SHEET 64

EFF	AUTHORITY	ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



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DSGN LL	05/12/95
APPD JGW	3/4/96
NEXT HIGHER ASSY. -	
14:06:58	26-Feb-96

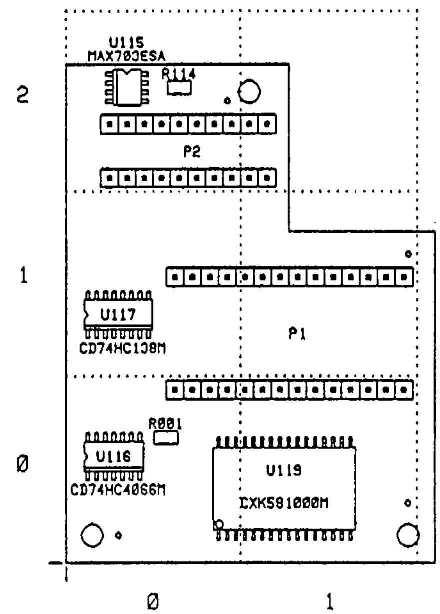
LUDLUM MEASUREMENTS INC

TITLE: 64K MEMORY EXPANDER BOARD

BOARD# 5371-054

SIZE	MODEL	SERIES	SHEET
D	2350-1	371	50

S0371054 SHEET 1 OF 1



LUDLUM MEASUREMENTS INC. SWEETWATER, TX.				
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DSGN LL	05/12/95	MODEL 2350-1	SERIES 371	SHEET S1
APP JGW	3/4/96	COMP ARTWORK ☐	SLDR ARTWORK ☐	
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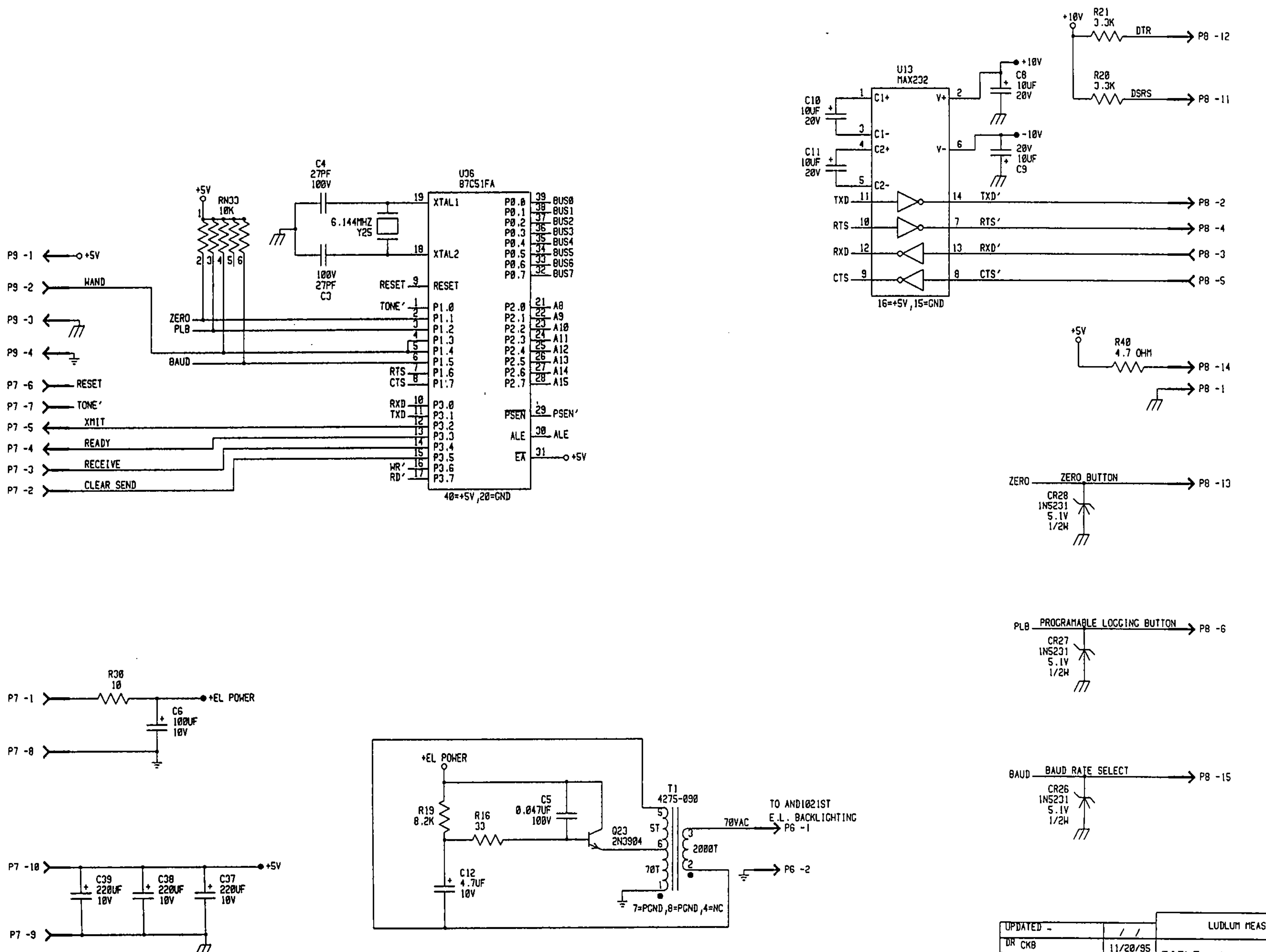

EFF	AUTHORITY	ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED

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CHK R.C.	3/4/96	
DSGN RSS	11/20/95	BOARD# 5371-063
APPD JGW	3/4/96	SIZE D · MODEL 2350-1 · SERIES 371 · SHEET 58
NEXT HIGHER ASSY. -		
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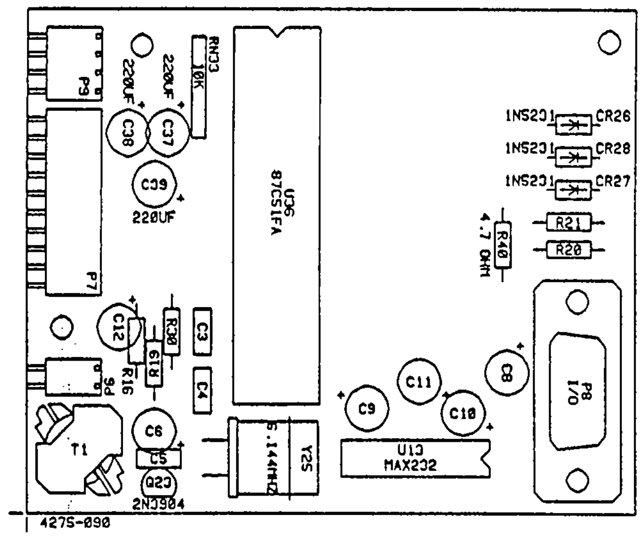

LUDLUM MEASUREMENTS INC.			SWEETWATER, TX.		
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APP	JGW	3/4/96	COMP ARTWORK ☐	SLDR ARTWORK ☐	
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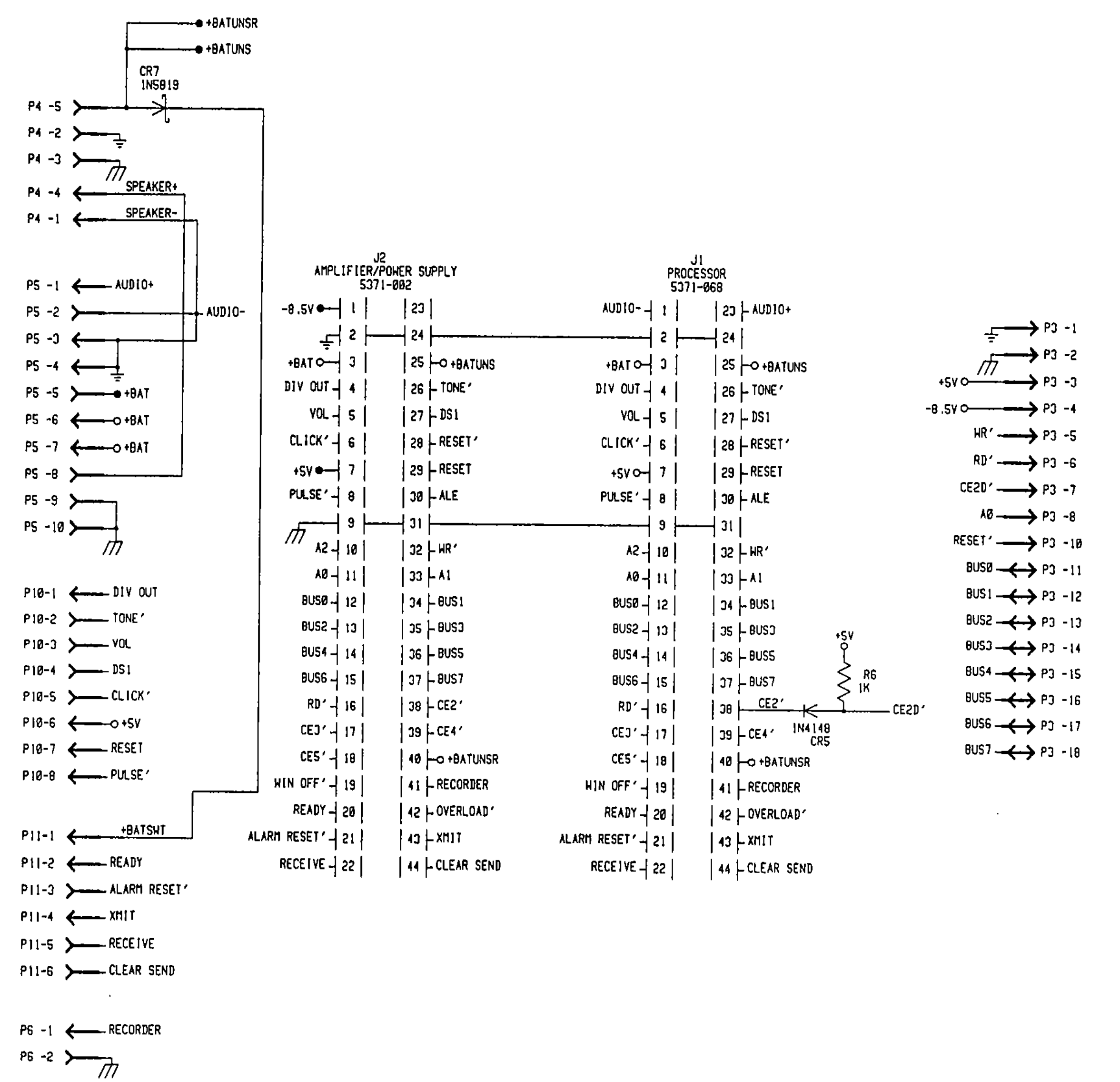
EFF	AUTHORITY	ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



UPDATED -	/ /	LUDLUM MEASUREMENTS INC.	
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CHK JSS	9/17/96		
DSGN LL	9/27/88	BOARD# 5371-003	
APPD JBW	9/17/96	SIZE D · MODEL 2350-1	SERIES 371 · SHEET 3
NEXT HIGHER ASSY. -			
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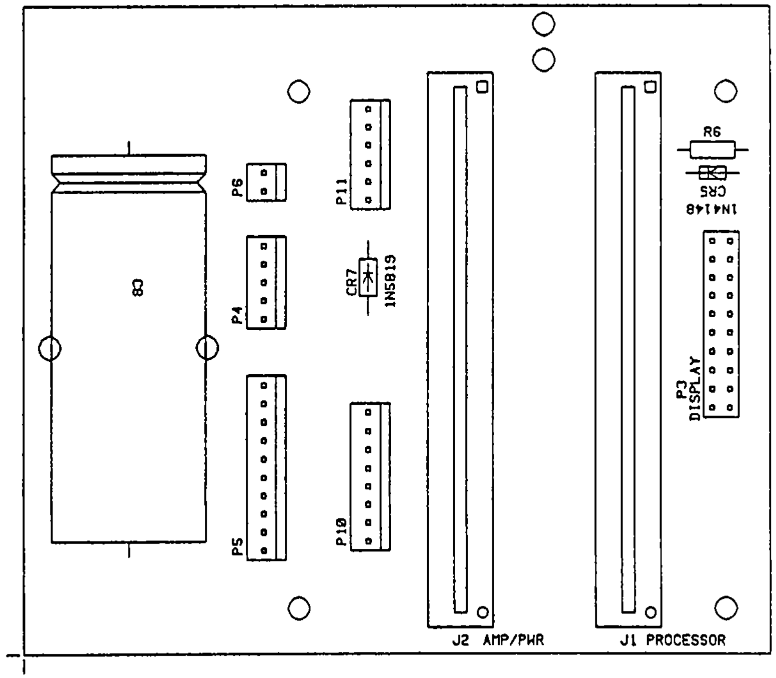

LUDLUM MEASUREMENTS INC. SWEETWATER, TX.			
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DSGN LL	10/20/88	MODEL 2350 SERIES 371	SHEET 29
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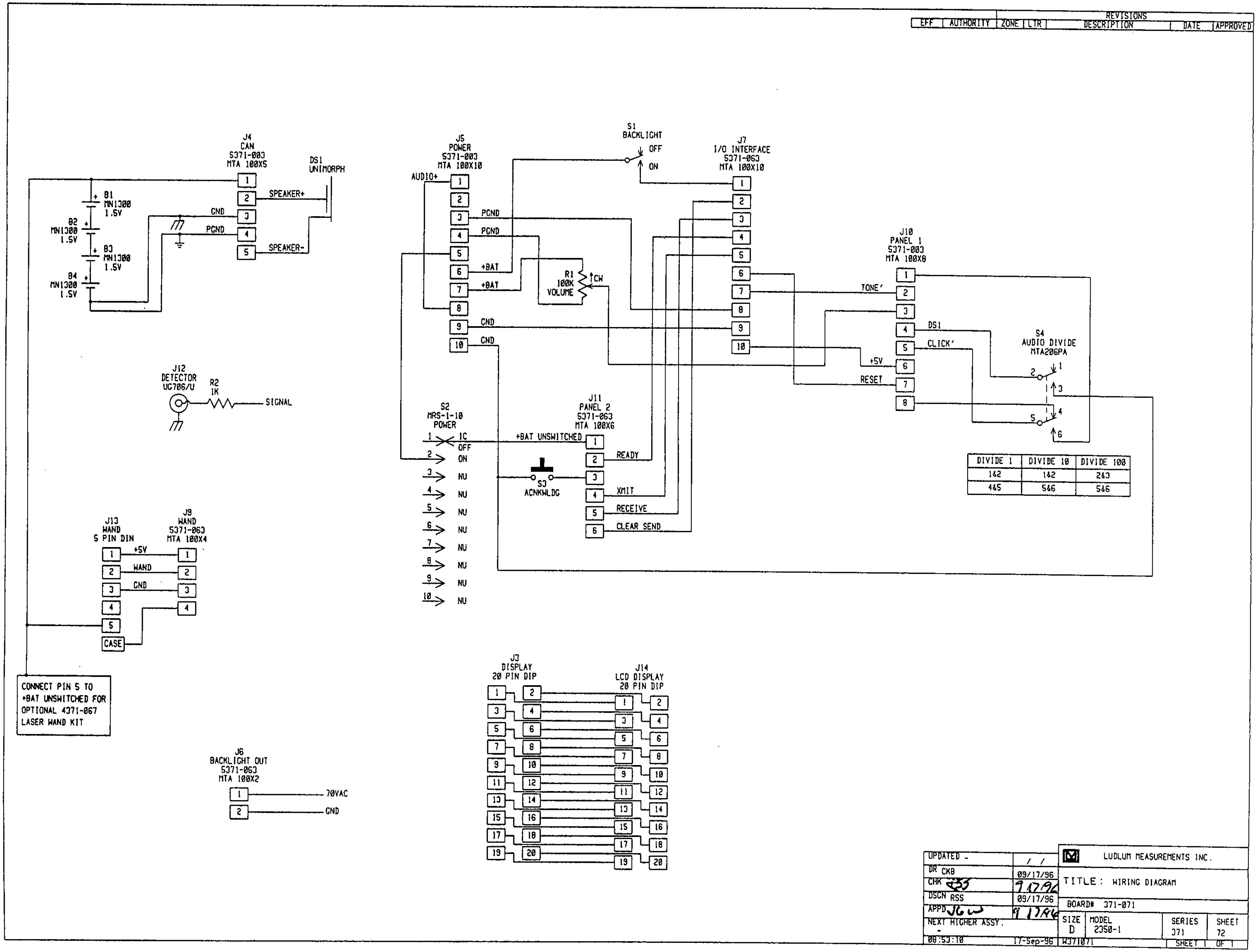

DIVIDE 1	DIVIDE 10	DIVIDE 100
1&2	1&2	2&3
4&5	5&6	5&6